IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (original): A computer system, comprising:
   a graphics accelerator unit which manages page faulting of texture data invisibly to the host processor.

2. (original): A computer system, comprising:
   a graphics accelerator unit which manages page faulting of texture data, from dedicated graphics memory into a main memory used by at least one host processor, invisibly to the host processor, except when said graphics accelerator unit calls for data which has not recently been present in said main memory.

3. (original): A computer system, comprising:
   at least one CPU, operatively connected to have read/write access to a main memory;
   first memory management logic, which virtualizes said main memory with reference to at least one bulk storage unit; and
   a graphics accelerator unit, comprising rendering accelerator logic, dedicated graphics memory, and a second memory management unit which manages texture data for said accelerator logic and performs page faulting of said texture data, invisibly to said CPU.

4. (previously presented): A computer system comprising:

a host processor having respective physical memory associated therewith; and

a graphics accelerator unit having respective local memory associated therewith, and also having a graphics memory manager;

wherein, when said graphics accelerator unit attempts to access texture data which is in said physical memory associated with said host, said graphics memory manager fetches said texture data automatically.

5. (previously presented): The system of Claim 4, wherein, after fetching said texture data, said graphics memory manager restarts texture processing.

6. (canceled)

7. (previously presented): A computer system comprising:

a host processor having host physical memory associated therewith, and also having virtual memory management; and

a graphics accelerator unit having respective physical memory associated therewith, and also having virtual memory management; and

wherein, when said graphics accelerator unit attempts to access texture data which is in said host physical memory,

if said texture data is in said host physical memory, said graphics memory manager fetches said texture data therefrom automatically;

and if said texture data is not in said host physical memory, said texture data is first loaded into said host physical memory, and thereafter said graphics memory manager fetches said texture data automatically from said host physical memory.

8. (previously presented): The system of Claim 2, wherein said graphics accelerator unit also includes a PCI/AGP interface, DMA controllers, SGRAM/SDRAM, a RAMDAC, and a video stream interface.

9. (previously presented): The system of Claim 2, wherein said dedicated graphics memory is SGRAM/SDRAM to which the unit has read-write access through its frame buffer and local buffer ports.

10. (previously presented): The system of Claim 2, wherein said host processor is operatively connected to receive inputs from input devices through an interface manager chip which provides an interface to various ports and registers.

11. (previously presented): The system of Claim 3, wherein said CPU includes a user input device, a microprocessor, and a data output device.

12. (previously presented): The system of Claim 3, wherein said first memory management logic is a bridge controller.

13. (previously presented): The system of Claim 3, wherein said bulk storage unit is a mass storage disk drive.

14. (**currently amended**): A computer system, comprising:

at least one CPU, operatively connected to have read/write access to a main memory;

first memory management logic, which virtualizes said main memory with reference to at least one bulk storage unit; and

a graphics accelerator unit, comprising rendering accelerator logic, dedicated graphics memory, and a second memory management unit which manages texture data for said accelerator logic and performs page faulting of said texture data, invisibly to said CPU;

[[The system of Claim 3,]]wherein said graphics accelerator unit also includes a PCI/AGP interface, DMA controllers, SGRAM/SDRAM, a RAMDAC, and a video stream interface.

15. (**currently amended**): A computer system, comprising:

at least one CPU, operatively connected to have read/write access to a main memory;

first memory management logic, which virtualizes said main memory with reference to at least one bulk storage unit; and

a graphics accelerator unit, comprising rendering accelerator logic, dedicated graphics memory, and a second memory management unit which manages texture data for said accelerator logic and performs page faulting of said texture data, invisibly to said CPU;

[[The system of Claim 3,]]wherein said second memory management unit also manages texture storage in the main memory in addition to managing texture storage in normal texture memory.

16. (previously presented): The system of Claim 4, wherein said host processor is operatively connected to receive inputs from input devices through an interface manager chip which provides an interface to various ports and registers.

17. (**currently amended**): A computer system comprising:

a host processor having respective physical memory associated therewith; and

a graphics accelerator unit having respective local memory associated therewith, and also having a graphics memory manager;

wherein, when said graphics accelerator unit attempts to access texture data which is in said physical memory associated with said host, said graphics memory manager fetches said texture data automatically; and

[[The system of Claim 4,]]wherein said graphics accelerator unit also includes a PCI/AGP interface, DMA controllers, SGRAM/SDRAM, a RAMDAC, and a video stream interface.

18. (previously presented): The system of Claim 4, wherein said graphics memory manager comprises:

means for determining where a page is located in host physical memory;

means for updating page tables for said page;

means for downloading said page; and

means for restarting texture processing.

19. (previously presented): The system of Claim 7, wherein said host processor is operatively connected to receive inputs from input devices through an interface manager chip which provides an interface to various ports and registers.

20. **(currently amended)**: A computer system comprising:

a host processor having host physical memory associated therewith, and also having virtual memory management; and

a graphics accelerator unit having respective physical memory associated therewith, and also having virtual memory management; and

wherein, when said graphics accelerator unit attempts to access texture data which is in said host physical memory,

if said texture data is in said host physical memory, said graphics memory manager fetches said texture data therefrom automatically;

and if said texture data is not in said host physical memory, said texture data is first loaded into said host physical memory, and thereafter said graphics memory manager fetches said texture data automatically from said host physical memory; and

[[The system of Claim 7,]]wherein said graphics accelerator unit also includes a PCI/AGP interface, DMA controllers, SGRAM/SDRAM, a RAMDAC, and a video stream interface.